UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,168	07/09/2001	Akira Kamiya	2001_0976A	5407

513 7590 08/05/2004

WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
LEE, RICHARD J	

ART UNIT	PAPER NUMBER
2613	6

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,168	KAMIYA, AKIRA	
	Examiner	Art Unit	
	Richard Lee	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Kawakami of record (6,332,058).

Kawakami discloses an information reproduction apparatus as shown in Figures 1 and 2, and the same multiple decoding method as claimed in claim 5, in which a signal is composed of a plurality of encoded data is inputted, to simultaneously decode two or more of the data (see Figures 1 and 2), comprising the same inputting the signal and extracting the two or more data to be decoded and reproduced (i.e., 18 of Figures 1 and 2); storing the extracted data in a buffer (i.e., 30 of Figure 1); distributing the data stored in the buffer (i.e., as provided by 40 of Figure 2 and see column 5, lines 46-54, column 7, lines 7-18) for each type (i.e., the MPEG stream of data as shown in Kawakami is based according to a specific type of video which includes inherent and specific header data, see column 5, lines 46-54, column 7, lines 7-18) and respectively storing the data in a plurality of separate buffers (i.e., 34 of Figure 2); controlling output of data stored in the plurality of separate buffers such that the data stored in the plurality of separate buffers are associated with each other (i.e., as provided by 32 of Figure 2 and see column 5, lines 31-45); and decoding, responsive to the controlling, the data stored in the plurality of separate

buffers and outputting the decoded data (i.e., as provided by 22 of Figure 2, and see column 5, lines 31-45).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami as applied to claim 5 in the above paragraph (2), and further in view of Siong et al of record (6,028,632).

Kawakami and substantially the same multiple decoding apparatus receiving a signal composed of a plurality of encoded data for simultaneously decoding two or more of the data (see Figures 1 and 2) as claimed in claim 1, comprising substantially the same reproduction controller (i.e., 24, 36 of Figure 2) for outputting various types of control information related to decoding and reproduction of the data; a date extractor (i.e., MPEG core server 18 of Figures 1 and 2) for receiving the signal for extracting the two or more data designate by the control information; a buffer (i.e., 20, 30 of Figure 2) storing the data extracted by the data extractor; a buffer manager (i.e., within core server 18 of Figures 1 and 2, and see column 5, lines 1-30) for controlling the buffer in accordance with the control information for the buffer; a data flow controller (i.e., 40 of Figure 2 and see column 5, lines 46-54, column 7, lines 7-18) for distributing the data stored in the buffer for each type and transferring the data in accordance with provided transfer conditions; a plurality of separate buffers (i.e., 34 of Figure 2) for respectively storing the data distributed and transferred by the data flow controller; a plurality of

decoders (i.e., 22 of Figures 1 and 2) respectively corresponding to the plurality of separate buffers for decoding the data stored in the separate buffers and outputting the decoded data; and a decoding controller for selecting a separate buffer and a decoder (i.e., CPU group 36 outputs control signal 38 in response to a request from external controller 24, thereby selecting the desired information for decoding to the respective buffer and decoder, see column 5, lines 46-54, column 7, lines 7-38) which are used for the decoding, from among the plurality of separate buffers and the plurality of decoders in accordance with the control information, and outputting information related to the separate buffer selected by the decoding controller, the transfer conditions based on the separate buffer selected by the decoding controller, and an instruction to start the decoding, respectively, to the separate buffer manager, the data flow controller, and the decoder selected by the decoding controller (i.e., controller 24 and CPU group 36 controls all the hardware structures, see columns 5-7).

Kawakami does not particularly disclose, though, a separate buffer manager for controlling the outputs of the plurality of separate buffers so as to be associated with each other in accordance with information for specifying the plurality of separate buffers as claimed in claim 1. It is noted that Kawakami does teach the particular use of a plurality of buffer managers (i.e., 32 of Figure 2) for controlling the outputs of each of the respective plurality of separate buffers 34, but and not particularly a separate buffer manager for controlling the outputs of the plurality of separate buffers as claimed. However, Siong et al discloses a multiple buffer and video decoder management system as shown in Figure 1, and teaches the general concept of the use of a separate buffer manager (i.e., 6 of Figure 1 and see column 3, line 56 to column 4, line 27) for controlling outputs of the plurality of separate buffers (i.e., 7-9 of Figure 1). Therefore, it

would have been obvious to one of ordinary skill in the art, having the Kawakami and Siong et al references in front of him/her and the general knowledge of buffer management systems, would have had no difficulty in providing the separate buffer manager of Siong et al in place of the plurality of separate buffer managers 32 of Kawakami for the same well known single unit integrated processing and so that less hardware would be required for managing the buffers purposes as claimed.

5. Claims 2-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami and Siong et al as applied to claims 1 and 5 in the above paragraphs (2) and (4), and further in view of Haskell et al of record (5,159,447).

Kawakami discloses substantially the same multiple decoding apparatus and method as above, but does not particularly disclose, though, the followings:

(a) the buffer manager outputs, when the buffer becomes full of the data, an overflow notification to the reproduction controller; the reproduction controller outputs, upon receipt of the overflow notification, an instruction to stop the data extraction to the data extractor, and outputs an initialization instruction to the decoding controller; the decoding controller outputs, upon receipt of the initialization instruction from the reproduction controller, an instruction to initialize all of the plurality of separate buffers to the separate buffer manager, outputs to the buffer manager an instruction to initialize the buffer, and respectively outputs instructions to stop the decoding to all of the plurality of decoders; the buffer manager initializes the buffer in accordance with the initialization instruction from the decoding controller; the separate buffer manager initializes all the plurality of separate buffers in accordance with the initialization

instruction from the decoding controller; and all the processing which is stopped is resumed after all the buffer and the plurality of separate buffers are initialized as claimed in claim 2;

(b) the separate buffer manger outputs, when a specific separate buffer becomes full of the data, an overflow notification that the specific separate buffer overflows to the decoding controller, the decoding controller outputs, upon receipt of the overflow notification that the separate buffer overflows, an instruction to stop the data transfer to the specific separate buffer to the data flow controller, an instruction to discard the data directed toward the specific separate buffer to the data flow controller, outputs an instruction to stop the decoding to a decoder corresponding to the specific separate buffer, and outputs to the separate buffer manager an instruction to initialize the specific separate buffer, the separate buffer manager initializes the specific separate buffer in accordance with the initialization instruction from the decoding controller, and all the processing which is stopped is resumed, and the discard of the data is released after the specific separate buffer is initialized as claimed in claims 3 and 4;

(c) when the buffer becomes full of the data, stopping extraction and decoding of the data, initializing all of the buffer and the plurality of separate buffers, and resuming all the processing which is stopped after all of the buffer and the plurality of separate buffers are initialized; when a specific separate buffer becomes full of the data, discarding the data directed toward the specific separate buffer, stopping the distribution of the data into the specific separate buffer and the decoding of the data stored in the specific separate buffer, initializing the specific separate buffer, and resuming all the processing which is stopped after the specific separate buffer is initialized, and releasing the discard of the data as claimed in claims 6-8.

Regarding (a) to (c), Haskell et al discloses a buffer control for variable bit rate channel as shown in Figures 1-4, and teaches the conventional notification of overflow situations associated with encoder and decoder buffers (see column 17, line 66 to column 18, line 13), and the particular termination of packets of data within the decoder as one way of preventing overflow in the buffers, thereby stopping decoding to the decoder, data extraction, data transfer to the specific buffer, and discarding data directed toward the specific buffer (see column 16, lines 27-39). It is noted that Haskell et al is however silent as to the initialization of the respective buffer components in response to the overflow notification and the subsequent resuming of the processing which was stopped after buffer initialization and the discard of the data is released after the buffer is initialized as claimed. But, it is considered obvious even without specific disclosure that once the packets are terminated within Haskell due to buffer overflow, the buffers of Haskell must be initialized since the existing data within the buffers are of no use and so that the buffers could be properly re-set. Further, after such buffer initialization and re-setting within Haskell, all processing will therefore be resumed, and the discarded data is released (i.e., the existing data in the buffer is of no use and therefore is released) after buffer initialization. Therefore, it would have been obvious to one of ordinary skill in the art, having the Kawakami, Siong et al, and Haskell et al references in front of him/her and the general knowledge of video encoder and decoder buffer fullness, would have had no difficulty in providing the overflow notification, termination of packets of data within the decoder as one way of preventing overflow in the buffers, thereby stopping decoding to the decoder, data extraction, data transfer to the specific buffer, and discarding data directed toward the specific buffer as taught by Haskell as well as the obvious initialization of buffers upon receipt of an overflow

notification and the subsequent resuming of the processing which was stopped after buffer initialization and the discard of the data is released after the buffer is initialized within Haskell for the multiple decoder of Kawakami so that the buffer manager, reproduction controller, decoding controller, and separate buffer manager of Kawakami may proper respond to the overflow notification for the same well known video decoder buffer overflow protection purposes as claimed.

6. Regarding the applicant's arguments at pages 10-11 of the amendment filed May 25, 2004 concerning in general that "...The data flow controller of independent claim 1 is required to be operable to distribute that data stored in the buffer and to transfer the data in accordance with "provided transfer conditions." Kawakami fails to teach the above identified limitation ... Kawakami describes that the time-divisional multiplexing controller 40 controls the timing of reading out information materials from DMA buffers. Accordingly, the time-divisional multiplexing controller 40 of Kawakami distributes data based on timing. As a result, Kawakami is required to solve a problem ... In order to solve the problem, the time-divisional multiplexing controller 40 of Kawakami is required to supply effective flags EF to corresponding gate controllers so as to permit only effective information materials (that are desired to be used) to be captured by the corresponding decoder buffers. The data flow controller of the present application is not required to perform such an operation ...", the Examiner wants to point out that though the time-divisional multiplexing controller 40 of Kawakami distributes data based on timing and supplies effective flags EF to the gate controllers, Kawakami is still nevertheless concerned with the distributing of data stored in the buffer for each type and transferring the data in accordance with provided transfer conditions, as claimed. The applicant's attention is directed

to column 7, lines 7-11 of Kawakami for the particular teachings of "the time-divisional multiplexing controller 40 is to control reading of information materials from the DMA buffers 30 so as to cause a desired information material 14 to flow through the MPEG stream bus SB at a desired time point". It is submitted that the MPEG stream of data as shown in Kawakami is based according to a specific type of video which includes inherent and specific header data that must be transferred according with provided transfer conditions. And since the multiplexing controller 40 of Kawakami controls the reading and transfer of the MPEG stream of data at a desired time point, it is submitted that such desired time point also reads on the provided transfer conditions as claimed.

Regarding the applicant's arguments at pages 11-12 of the amendment filed May 25, 2004 concerning in general that Kawakami fails to teach "separate buffer manager for controlling outputs of said plurality of separate buffers so as to associate with each other in accordance with information for specifying said plurality of separate buffers", since the gate controller 32 of Kawakami is provided for each decoder buffer 34, with each gate controller 32 able to control only one decoder buffer 34, the Examiner wants to point out that such arguments are deemed moot in view of the above new grounds of rejections.

Regarding the applicant's arguments at pages 12-13 of the amendment filed May 25, 2004 concerning in general that "... Kawakami does not include any description about an element corresponding to the decoding controller of the present application ... Therefore, Kawakami fails to teach a decoding controller for selecting a separate buffer and a decoder from among a plurality of separate buffers and a plurality of decoders as required in independent claim 1 ...", the Examiner respectfully disagrees. It is submitted again that the CPU group 36 of

Kawakami, by outputting a control signal 38 in response to a request from external controller 24 to select the desired information for decoding to the respective buffer and decoder (see column 5, lines 46-54, column 7, lines 7-38), reads on the claimed features of a decoding controller for selecting a separate buffer and a decoder from among a plurality of separate buffers and a plurality of decoders.

Regarding the applicant's arguments at page 13 of the amendment filed May 25, 2004 concerning in general that "... The decoder buffer 34 of Kawakami does not distribute data stored in a HDD 20 and a KMA buffer 30 by data type. In Kawakami, the gate controller 32 distributes the data stored in the HDD 20 and the DMA buffer 32. However, the distributing of claim 5 does not correspond to an operation of the gate controller 32 of Kawakami. In particular, the distributing of claim 5 is performed by the data flow controller ...", the Examiner wants to point out that element 40 of Kawakami is being relied upon for the particular features of distributing the data stored in the buffer 20, 30 for each type (i.e., the MPEG stream of data as shown in Kawakami is based according to a specific type of video which includes inherent and specific header data, see column 5, lines 46-54, column 7, lines 7-18) and respectively storing the data in a plurality of separate buffers 34 of Figure 2. The particular step of distributing the data stored in the buffer as claimed is therefore anticipated by Kawakami.

At page 14 of the amendment filed May 25, 2004, the applicant argues in general that Haskell fails to teach stopping decoding to a decoder, stopping data extraction and discarding data directed toward specific buffer as required in claims 2-4, and column 16, lines 27-39 of Haskell merely describes that a current packet is terminated in order to prevent overflow of buffers. It is submitted that the particular termination of a current packet to a buffer within a

video decoder as taught Haskell et al (see column 16, lines 27-39) nevertheless reads on the stopping decoding to a decoder, stopping data extraction and discarding data directed toward the specific buffer as claimed.

Regarding the applicant's arguments at pages 14-15 of the amendment filed May 25, 2004 concerning in general limitations claimed in claims 1 and 5, the Examiner wants to point out that such arguments have been addressed in the above.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications; please mark "EXPEDITED PROCEDURE") (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Lee whose telephone number is (703) 308-6612. The Examiner can normally be reached on Monday to Friday from 8:00 a.m. to 5:30 p.m, with alternate Fridays off.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group customer service whose telephone number is (703) 306-0377.

RICHARD LEE
PRIMARY EXAMINER

Richard Lee/rl

8/3/04